Network serial port transparent transmission chip CH9121

Datasheet

Version: V2.5

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1. Overview

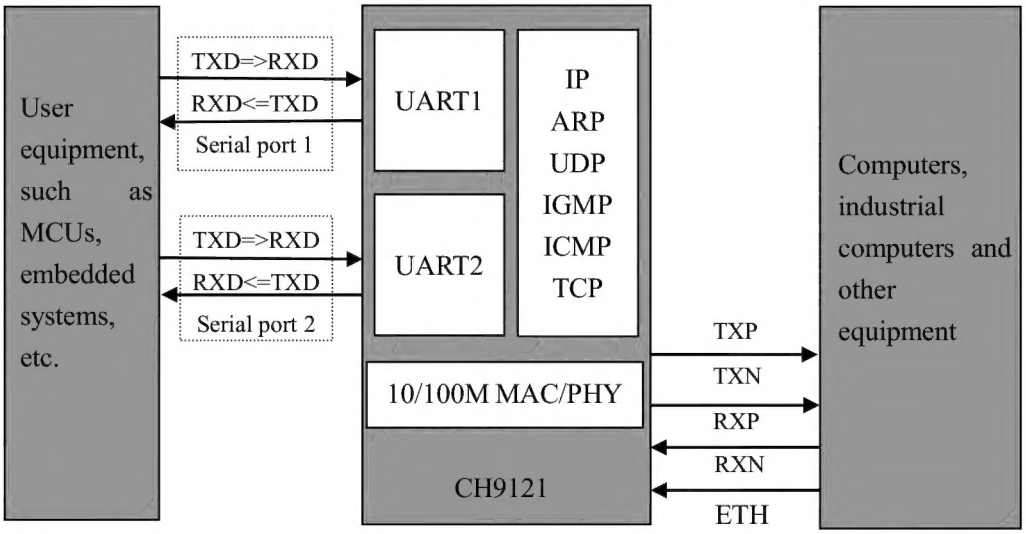
CH9121 is a network serial port transparent transmission chip with built-in 10/100M Ethernet media transmission layer (MAC) and physical layer (PHY), fully compatible with IEEE802.3 protocol. It integrates TCP/IP protocol stack internally, which can realize bidirectional transparent transmission of network data packets and serial port data.

CH9121 has 4 working modes: TCP CLIENT, TCP SERVER, UDP CLIENT and UDP server, and the highest baud rate of serial port can support 10Mbps.

Users can easily configure parameters through PC software or serial commands. Users are advised to use the upper computer software for configuration. If you need to use the serial command configuration, please refer to the document *CH9121 Serial Control Command. PDF* in CH9121EVT.

The following figure shows the application block diagram of CH9121.

Table 1-1 CH9121 application block diagram

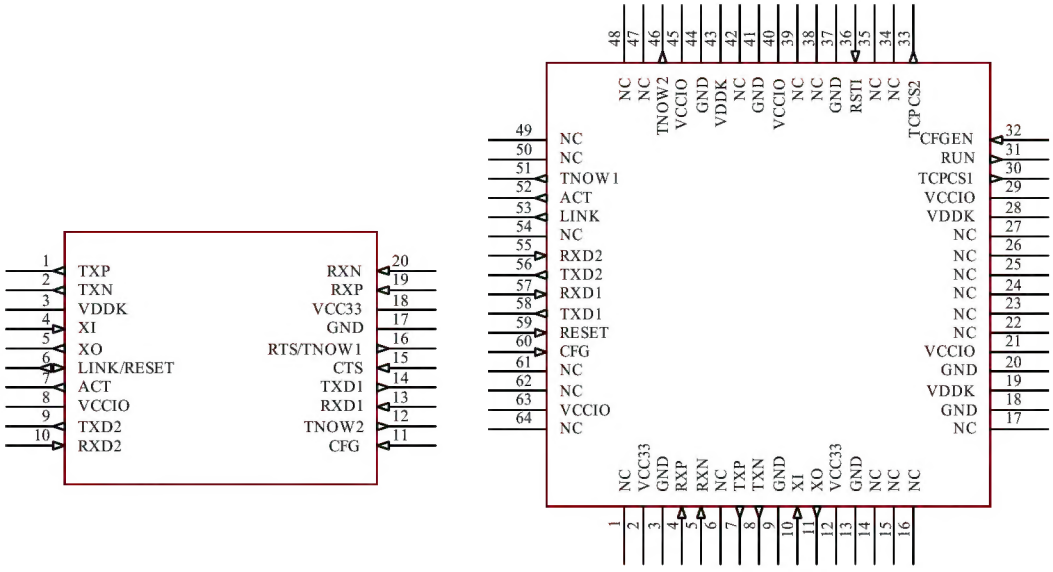


2. Features

- Built-in Ethernet media transmission layer MAC and physical layer transceiver PHY
- Support 10/100M, full-duplex/half-duplex adaptive, compatible with IEEE 802.3 protocol.
- Support automatic conversion of MDI/MDIX lines
- The I/O port supports 3.3V, 2.5V, and 1.8V power supply, and is compatible with microcontrollers of various voltage standards
- Built-in network port pull-up resistor, crystal oscillator matching capacitor, simplifying external circuit
- Built-in TCP/IP protocol cluster, supporting IPv4, ARP, ICMP, IGMP, UDP and TCP protocols.
- Support DHCP to automatically obtain IP address and DNS domain name access.
- Support TCP CLIENT, TCP SERVER and UDP CLIENT, UDP SERVER 4 working modes
- Support 2 independent serial ports and independent transparent transmission
- The serial port baud rate supports 300 bps to 10Mbps.

- Support setting chip working mode, port, IP and other network parameters through host computer software and serial port commands
- The serial port supports full-duplex and half-duplex serial communication, and supports RS485 automatic switching of transmitting and receiving
- Provide LED status display Link and ACT.
- Provide computer-side virtual serial port software
- Support KEEPALIVE mechanism
- TSSOP20 and LQFP64M lead-free packages are available.

3. Pinouts



CH9121T CH9121A

Table 3-1 Package Description

Package Form	Body Size	Pin Pitch		Package Description	Order Model
TSSOP20	4.4*6.5mm	0.65mm	25.6mil	Thin Shrink Small Outline Package	CH9121T
LQFP64M	10*10mm	0.5mm	19.7mil	Low-profile Quad Flat Package	CH9121A

Note:

1. For new designs, it is recommended to use CH9121T, which supports hardware flow control, has a smaller package, and has a more streamlined peripheral circuit.

2. CH9121A is upgraded based on the previous version CH9121 (without suffix letters), and the pins are basically compatible. The peripheral circuit needs to be adjusted when replacing.

3. The previous version CH9121 (without suffix letters) is still available but is not recommended for new designs.

4. Pin Definitions

Table 4-1 CH9121T Pin definitions

CH9121T Pin No.	Pin name	Type	Pin description
1	TXP	I/O	Differential output in 10BASE-T/100BASE-TX MDI mode; Differential input in 10BASE-T/100BASE-TX MDIX mode.
2	TXN		
19	RXP	I/O	Differential input in 10BASE-T/100BASE-TX MDI mode; Differential output in 10BASE-T/100BASE-TX MDIX mode.
20	RXN		
3	VDDK	P	Place an external 1uF ground capacitor close to the chip.
18	VCC33	P	For 3.3V main power input, it is recommended to place a 0.1uF capacitor in parallel with a 10uF or 4.7uF capacitor close to the chip.
8	VCCIO	P	For the power input of the I/O interface, it is recommended to place a 0.1uF ground capacitor close to the chip.
17	GND	P	Common ground terminal.
4	XI	I	Crystal oscillator input, requires an external 25MHz crystal, or external clock input, with built-in crystal matching capacitor.
5	XO	O	Crystal oscillator inverts and needs to be connected to the other end of an external 25MHz crystal. It has a built-in crystal matching capacitor.
6	LINK/RESET	I/O,PU	Alternate pin, built-in pull-up resistor, detect pin level during power-on. Low level selects RESET function, floating or high level selects LINK function. LINK network connection indicator LED output: Low level indicates that the Ethernet PHY is connected; High level indicates that the Ethernet PHY is not connected. RESET control input (restore factory settings): If the detection pin is at a low level for 2 seconds during power-on, CH9121 will be restored to factory settings. After the pin returns to a high level, the LINK function will be enabled.
7	ACT	O	Carrier sensing indicator LED output: LED flashes to indicate carrier sensing signal.
9	TXD2	O	Serial port 2 data output.
10	RXD2	I,PU	Serial port 2 data input, built-in pull-up resistor.
11	CFG	I,PU	Serial port configuration mode setting pin, built-in pull-up resistor, when a low level is detected, it enters the serial port configuration mode, and exits the configuration mode when it is left floating or at a high level.
12	TNOW2	O	Transmit status output, used to control the RS485 transmitting and receiving switching of serial port 2.
13	RXD1	I,PU	Serial port 1 data input, built-in pull-up resistor.
14	TXD1	O	Serial port 1 data output.
15	CTS	I,PD	Clear transmit Input:

			If it is a high level, serial port 1 blocks the next data transmission when the current data transmission ends, and can be connected to the peer RTS to implement hardware flow control.
16	RTS/TNOW1	I/O,PU	Alternate pin with built-in pull-up resistor to detect pin level during power-on. An external pull-down resistor of about 4K7 makes this pin low during power-on and selects the TNOW1 function. If it is left floating or high during power-on, the RTS function is selected. RTS transmit request output: If it is a low level, it means that serial port 1 is ready to receive data and can be connected to the other end's CTS to implement hardware flow control. TNOW1 output: Transmitting status output, used to control the RS485 transmitting and receiving switching of serial port 1.

Table 4-2 CH9121A Pin definitions

CH9121A Pin No.	Pin name	Type	Pin description
4	RXP	I/O	Differential input in 10BASE-T/100BASE-TX MDI mode; Differential output in 10BASE-T/100BASE-TX MDIX mode.
5	RXN		
7	TXP	I/O	Differential output in 10BASE-T/100BASE-TX MDI mode; Differential input in 10BASE-T/100BASE-TX MDIX mode.
8	TXN		
2/12	VCC33	P	3.3V power supply input, it is recommended that 0.1uF parallel 10uF or 4.7uF ground capacitor be placed close to the chip.
19	VDDK	P	Place an external 1uF ground capacitor close to the chip.
28/43	VDDK	P	Place an external 0.1uF ground capacitor close to the chip.
21/29/40/45/63	VCCIO	P	For the power input of the I/O interface, it is recommended to place a 0.1uF ground capacitor close to the chip.
3/9/13/18/20/37/41/44	GND	P	Common ground terminal.
1/6/14/15/16/17/22/23/24/25/26/27/34/35/38/39/42/47/48/49/50/54/61/62/64	NC	-	Reserved, leave it suspended.
10	XI	I	Crystal oscillator input, requires an external 25MHz crystal, or external clock input, with built-in crystal matching capacitor.
11	XO	O	The crystal oscillator inverts and needs to be connected to the other end of an external 25MHz crystal. It has a built-in crystal matching capacitor.
30	TCPCS1	O	In TCP mode, port 1 connection status indication output, low level is valid.
31	RUN	O	CH9121 operation status indication output.
32	CFGEN	I,PU	Network configuration enable pin, built-in pull-up resistor, detects pin level when powered on, if it is low level when

			powered on, it is forbidden to configure CH9121 through the host computer.
33	TCPCS2	O	In TCP mode, port 2 connection status indication output, low level is valid.
36	RSTI	I,PU	External reset input, low level valid, built-in pull-up resistor.
46	TNOW2	O	Transmitting status output, used to control the RS485 transmitting and receiving switching of serial port 2.
51	TNOW1	O	Transmitting status output, used to control the RS485 receiving and receiving switching of serial port 1.
52	ACT	O	Carrier sensing indicator LED output: LED flashes to indicate carrier sensing signal.
53	LINK	O	Network connection indication LED output: low level indicates that the Ethernet PHY is connected, high level indicates that the Ethernet PHY is not connected.
55	RXD2	I,PU	Serial port 2 data input, built-in pull-up resistor.
56	TXD2	O	Serial port 2 data output.
57	RXD1	I,PU	Serial port 1 data input, built-in pull-up resistor.
58	TXD1	O	Serial port 1 data output.
59	RESET	I,PU	Built-in pull-up resistor, if the detection pin is low for 2 seconds during power-on, CH9121 will be restored to factory settings
60	CFG	I,PU	Serial port configuration mode setting pin, built-in pull-up resistor, when a low level is detected, it enters the serial port configuration mode, and a high level exits the configuration mode.

Note 1:

I = Input; O = Output;

I/O = Input/Output; P = Power;

PU = Built-in pull-up resistor.

5. Function Parameter Descriptions

5.1 Overview

CH9121 is a network serial port transparent transmission chip, which can realize bidirectional transparent transmission of serial port data and network data, supports TCPCLEINT/SERVER, UDPCLIENT/SERVER4 working modes, and the serial port baud rate supports a range of 300bps~10Mbps. Before use, the network parameters and serial port parameters of the chip need to be configured through the host computer software NetModuleConfig.exe or serial port commands. After the configuration is completed, CH9121 saves the configuration parameters to the internal storage space. After the chip is reset, CH9121 will work according to the saved configuration values.

5.2 Basic Parameters

The basic parameters of CH9121 include: name, MAC address display, automatic IP address setting, manual IP address setting (including CH9121's IP address, subnet mask, default gateway), and serial port negotiation configuration.

Table 5-1 Basic parameters

Basic parameters	Description
Name	The name is mainly for the convenience of CH9121 chip management in the local area network, and the length does not exceed 20 bytes;
MAC address	Displays the MAC address of the currently selected chip;
Network parameter	There are 2 ways to set network parameters for CH9121: (1) DHCP, that is, automatically obtain network parameters from a gateway device with DHCP SERVER function; (2) Manually set the IP address, subnet mask, and default gateway.
Serial port negotiation configuration	The serial port negotiation configuration function can be turned on through the host computer, and the serial port configuration mode can be entered through the serial port handshake. It is closed by default.

5.3 Port Parameter

The CH9121 port parameters include: Network mode, local port, target IP/domain name, destination port, serial port baud rate/data bit/stop bit/check bit, network cable disconnection processing, RX package length, RX package timeout, and operation when the network is connected.

Table 5-2 Port parameter

Port parameter	Description
Network mode, local port, target IP/domain name, destination port	The network mode (TCPSERVER/CLIENT, UDPSERVER/CLIENT), destination IP address, and local/destination port are the basic parameters for network communication. The destination IP address can also be accessed via a domain name.
Serial port	The serial port baud rate range is 300bps to 10Mbps. CH9121 has 2 serial port reference clock modes. Users can modify the internal reference clock of the CH9121 serial port through the host computer software or command code to reduce the serial port communication error. The default mode of the CH9121 serial port reference clock is "Default", which can be adjusted to "Classical" according to needs. For details, refer to Section 6.1.1.

Network cable disconnection processing	When the network cable is disconnected, you can configure CH9121 to actively close the TCP connection internally or take no action.
RX packet length	The RX packet length range is 1 to 1024. When the CH9121 serial port receives data of the set length, the CH9121 will immediately package the serial port data and transmit it out through the network.
RX packet timeout	The timeout setting range is 0 to 200, and the unit time is approximately 5 milliseconds. For example, if the timeout value is set to 1, a serial port timeout will occur when the data length of the serial port receive buffer does not reach the RX package length and the serial port does not receive new data within 5ms. When the serial port timeout occurs, CH9121 will transmit the data received by the serial port through the network. When the timeout is set to 0, the internal hardware timeout (no new data is received for more than 4 data times) mechanism is enabled, which is suitable for occasions with high real-time requirements and large-volume data transmission and reception.
Network connection operation	The data received by the serial port before the TCP connection is established can be cleared (discarded) or retained when TCP is established.

5.4 Default Configuration

When CH9121 leaves the factory, port 2 is closed by default and port 1 works in TCPCLIENT mode by default. The default network parameters are shown in the table below.

Table 5-3 Default configuration

Default Configuration	Description
Device IP	192.168.1.200
Subnet mask	255.255.255.0
Default Gateway	192.168.1.1
Local port	2000
Destination IP	192.168.1.100
Destination port	1000
Serial port negotiation configuration	Off, do not allow entering serial port configuration mode through serial port handshake
Baud rate	9600
Data bit	8
Stop bit	1
Check	None
Network cable disconnection processing	Actively close the TCP connection
RX packet length	1024
RX packet timeout	0
Network connection operation	Do not clear the serial port buffer

6. Function Descriptions

6.1 UART

CH9121 provides 2 UARTs: Port 1 and port 2.

The UART signal lines include: serial data input pin RXD and serial data output pin TXD. CH9121T's serial port 1 also provides RTS and CTS for hardware automatic flow control at high baud rates. Through the serial interface, CH9121 can be connected point-to-point with MCU, DSP, or MCU with minimal wiring.

The baud rate error of the CH9121 serial port transmitting signal is less than 0.3%, and the allowable baud rate error of the serial port receiving signal is not more than 2%. The serial data format supports 5, 6, 7, 8 data bits and 1 or 2 stop bits, and supports odd parity, even parity, no parity, blank 0 parity and mark 1 parity. The default is the standard byte transmission mode, including 1 start bit, 8 data bits, 1 stop bit, and no parity. Users can modify it according to actual needs.

6.1.1 Serial Baud Rate

The default serial communication baud rate of CH9121 is 9600bps. The user can select the appropriate communication baud rate at any time through the host computer software or serial port command code. After the configuration is completed, CH9121 saves the baud rate parameters to the internal storage space. After the chip is reset, CH9121 will work at the saved baud rate.

CH9121 provides 2 serial port reference clock modes, the default mode is Default mode, users can select the appropriate serial port reference clock mode and baud rate according to the table below.

Table 6-1 Serial port reference clock and serial port baud rate selection

Baud rate (bps)	Serial port reference clock	
	Default mode (Default mode)	Classical mode
300	Available	Available
600	Available	Available
1200	Available	Available
2400	Available	Available
4800	Available	Available
9600	Available	Available
14400	Available	Available
19200	Available	Available
38400	Available	Available
57600	Available	Available
115200	Available	Available
230400	Available	Unavailable
460800	Available	Unavailable
921600	Available	Unavailable
1M	Unavailable	Available
2M	Unavailable	Available
5M	Unavailable	Available
10M	*Unavailable*	*Available*

Note: The 2 ports of CH9121 share a serial port reference clock. Users can set the two ports to different baud rates, but must ensure that both baud rates are available in the current serial port reference clock mode.

6.2 Other Hardware

CH9121 chip integrates 10M/100M Ethernet PHY, MAC, UART, SRAM, high-speed MCU, PLL frequency multiplier, power-on reset circuit, etc.

CH9121 chip has built-in power-on reset circuit, which can also be controlled by pulling RSTI pin low. RSTI pin of CH9121A is used to input asynchronous reset signal from outside; When the RSTI pin is low, the CH9121A chip is reset; When the RSTIA pin returns to the high level, CH9121A will enter the initialization phase for about 15ms, during which the host prohibits the operation of CH9121A.

7. Parameters

7.1 Absolute Maximum Value (Critical or exceeding the absolute maximum value will probably cause the chip to work improperly or even be damaged)

Table 7-1 Absolute maximum

Symbol	Parameter	Min.	Max.	Unit
T_A	Ambient temperature during operation	-40	85	℃
T_J	Junction temperature range	-40	100	℃
T_S	Ambient temperature during storage	-55	150	℃
V_{CC33}	Operating power supply voltage	-0.4	4.0	V
V_{CCIO}	I/O power supply voltage	-0.4	4.0	V
V_{DDK}	Power supply decoupling terminal for core analog circuits	-0.4	1.5	V
V_{ETH}	Voltage on ETH physical signal pin	-0.4	V_{CC33}+0.4	V
V_{IN}	Input voltage on pin	-0.4	V_{CCIO}+0.4	V
$V_{ESD(HBM)}$	ESD voltage (HBM) for common I/O pins	6K		V
I_{IO}	Sinking current on I/O pin		20	mA
	Output current on I/O pin		20	

7.2 Electrical Parameters

Table 7-2 Electrical Parameters (V_{CC33} = 3.3V, V_{CCIO} = 3.3V, T_A = 25℃)

Symbol	Parameter		Min.	Typ.	Max.	Unit
V_{CC33}	Operating power supply voltage		3.2	3.3	3.4	V
V_{CCIO}	I/O power supply voltage		1.7	3.3	3.6	V
V_{IL}	I/O pin, input low voltage	V_{CCIO} = 3.3V	0		0.8	V
		V_{CCIO} = 1.8V	0		0.6	
V_{IH}	I/O pin, input high voltage	V_{CCIO} = 3.3V	2.0		V_{CCIO}	V
		V_{CCIO} = 1.8V	1.2		V_{CCIO}	
V_{OL}	Low output voltage, single pin sinks 5mA			0.4	0.6	V
V_{OH}	High output voltage, single pin output 5mA		V_{CCIO}-0.6	V_{CCIO}-0.4		V
V_{hys}	I/O Schmitt trigger voltage hysteresis			150		mV
C_{IO}	I/O pin capacitance			5		pF
R_{PU}	Pull-up equivalent resistance		30	40	55	kΩ
R_{PD}	Pull-down equivalent resistor		30	40	55	kΩ
$t_{f(IO)out}$	Output high to low level fall time				6.5	ns
$t_{r(IO)out}$	Output low to high level rise time				11	ns

Note: The above parameters are guaranteed by design.

7.3 Power Consumption

Table 7-3 Power consumption (A_{VDD33} = 3.3V, V_{DDIO} = 3.3V, T_A = 25℃)

Symbol	Parameter	Conditions (All currents including network transformer)	Typ.	Unit
I_{DD0}	Supply current in transmission state	100BASE-TX channel is linked successfully and there are data packets on the transmit and receive channels.	76.1	mA
		10BASE-TX channel is linked successfully and there are data packets on the transmit and receive channels.	50.2	
I_{DD1}	Supply current in idle state	100BASE-TX channel is linked successfully and there are no packets on the transmit and receive channels.	76.2	mA
		10BASE-TX channel is linked successfully and there are data packets on the transmit and receive channels.	48.1	
I_{DD2}	Supply current in disconnected state	100BASE-TX and 10BASE-TX paths are not linked successfully and PHY is in auto-negotiation state.	55	mA

7.4 AC Electrical Characteristics and Timing

Table 7-4 Oscillator and crystal timing parameter table

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
TCKF	Crystal frequency	Recommended ≤ 30ppm	24.999	25	25.001	MHz
TPWH	Clock pulse width high		15	20	25	ns
TPWL	Clock pulse width low		15	20	25	ns

Note: The XI and XO pins have built-in 2 oscillation capacitors required by an external crystal with a load capacitance of 12pF, and only the crystal is required externally; if an external crystal with a load capacitance of 20pF is selected, then XI and XO need to add an additional 15pF oscillation capacitor to ground respectively.

Table 7-5 Reset timing parameters table

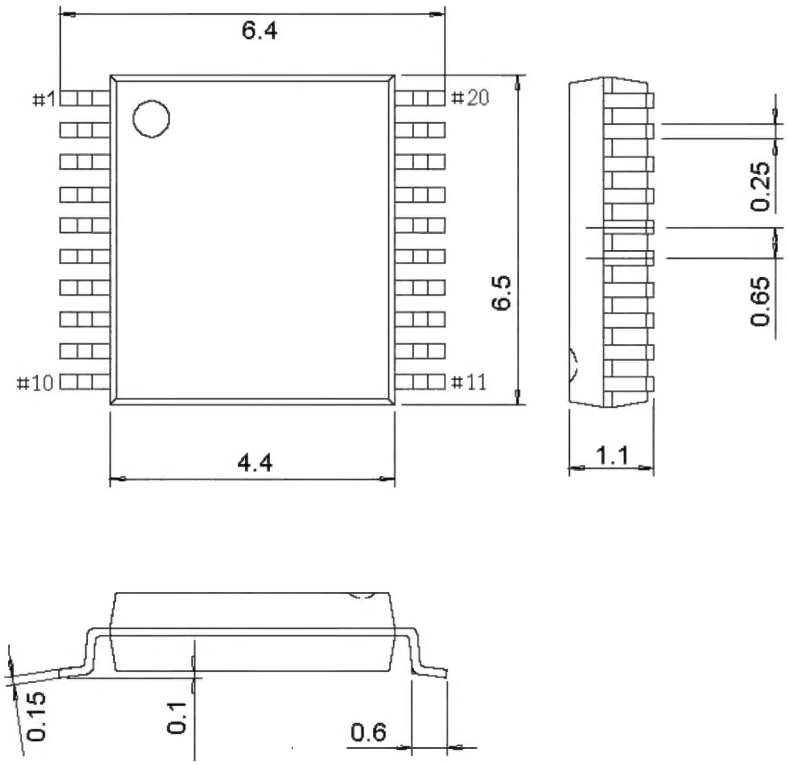
Symbol	Parameter	Min.	Typ.	Max.	Unit
$t_{RSTTEMPO}$	RSTI low level width	1			us
$t_{RSTTEMP1}$	RSTI high level to host can operate	11	15	19	ms
$t_{RSTTEMP2}$	Reset command valid to host operable	10	14	18	ms
$t_{RSTTEMP3}$	Power on reset to host operable	25	29	34	ms

8. Package Information

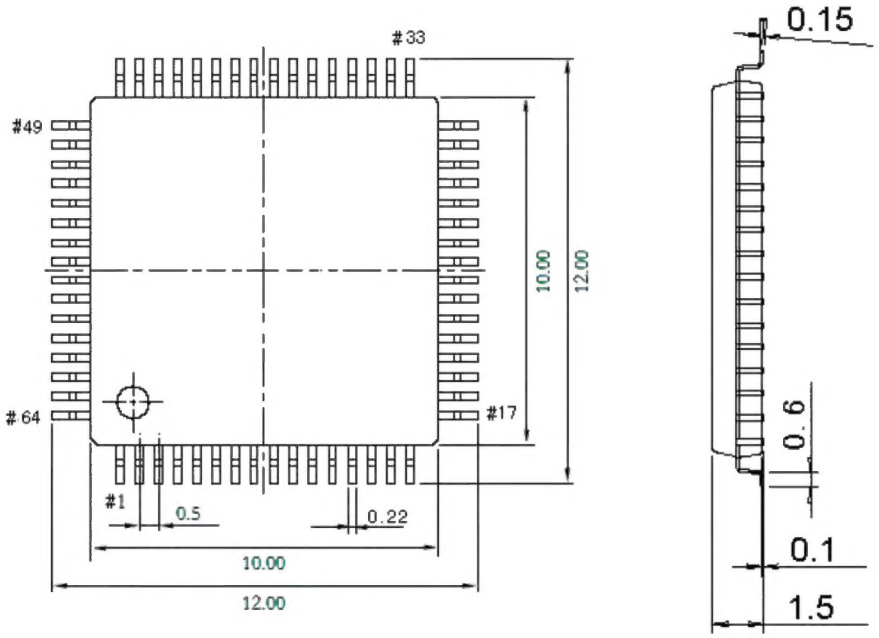
Note: All dimensions are in millimeters.

The pin center spacing values are nominal, without error. And the error of dimensions other than the pin center spacing values is not more than ±0.2mm.

8.1 TSSOP20



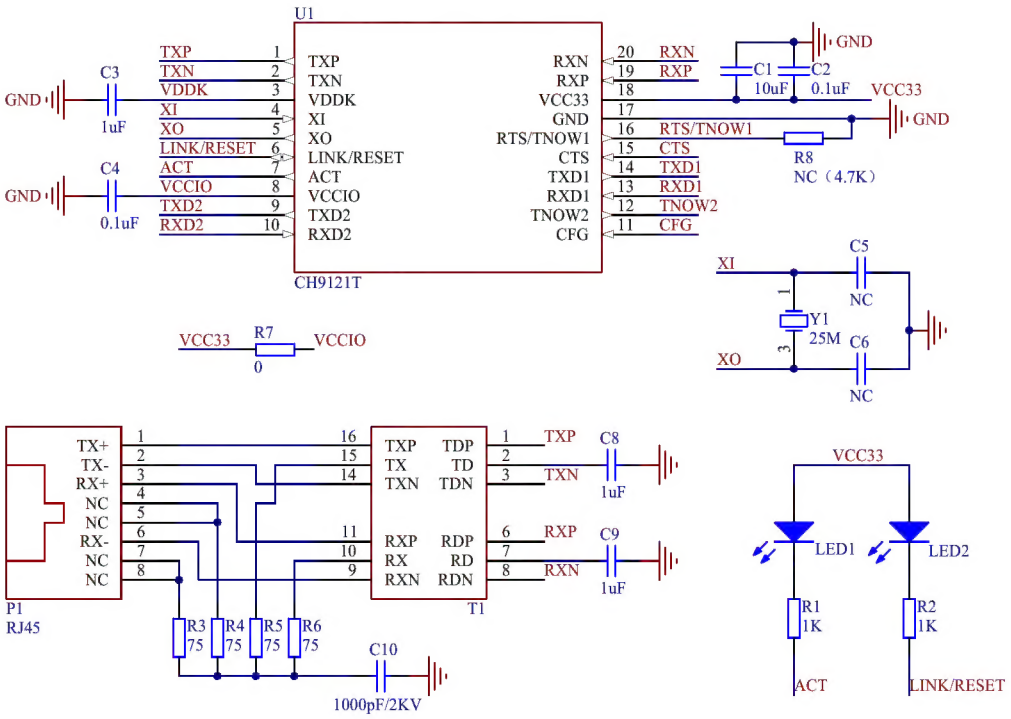
8.2 LQFP64M



9. Applications

9.1 CH9121T Reference Circuit

Figure 9-1 CH9121T hardware reference circuit



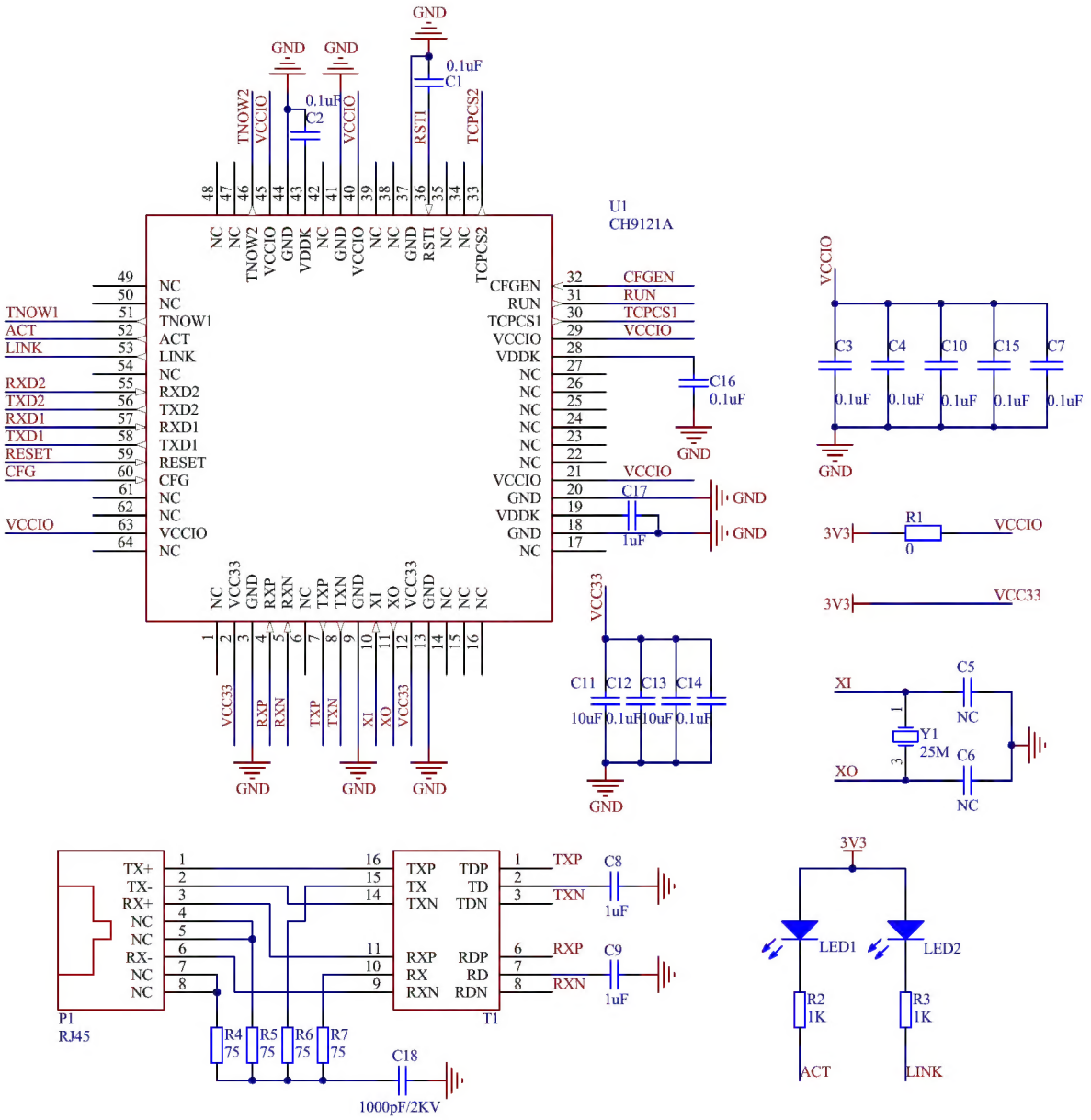
CH9121T has built-in part of the oscillation capacitance of crystal Y1, C5 and C6 can be adjusted according to the crystal parameters. For Y1 with a load capacitance of 12pF, C5 and C6 are not needed; for Y1 with a load capacitance of 20pF, C5 and C6 are recommended to be 15pF each.

CH9121T has built-in Ethernet 50Ω impedance matching resistor. Do not connect 49.9Ω or 50Ω resistor externally. It is equivalent to voltage drive.

T1 is an Ethernet network transformer, and its center tap is grounded through capacitors C8 and C9 respectively. Do not connect to any power supply.

9.2 CH9121A Reference Circuit

Figure 9-2 CH9121A hardware reference circuit



CH9121A has built-in part of the oscillation capacitance of crystal Y1, C5 and C6 can be adjusted according to the crystal parameters. For Y1 with a load capacitance of 12pF, C5 and C6 are not required; for Y1 with a load capacitance of 20pF, C5 and C6 are recommended to be 15pF each.

CH9121A has built-in Ethernet 50Ω impedance matching resistor, so do not connect 49.9Ω or 50Ω resistors externally, which is equivalent to voltage drive.

T1 is an Ethernet network transformer, and its center tap is grounded through capacitors C8 and C9 respectively. Do not connect to any power supply.

C3, C4, C7, C10, and C15 should be placed close to the VCCIO pins, and C11, C12, C13, and C14 should be configured in pairs, each group contains a 10uF and a 0.1uF capacitor, and are placed close to their respective VCC33 pins.

Upgrade from the previous version CH9121 (no suffix letter) to CH9121A, although both pins are basically compatible, but the network transformer and other peripheral circuit connections may need to be adjusted, please

refer to the relevant articles in the WCH official forum or contact technical support for specific changes.